K.S.R. COLLEGE OF ENGINEERING (Autonomous)

SEMESTER - V

BASICS OF VLSI DESIGN

L	T	P
3	0	0

Prerequisites: *Electronic Devices and Circuits, Digital Electronics*

Objectives: *Gain knowledge about MOS technology*

Learn about operation and characteristics of inverter and design rules.

Understand the concept of CMOS logic gate design and power dissipation

Gain knowledge about storage elements and different types of dynamic logic circuits

Familiarize Verilog programming concepts and coding types

INTRODUCTION TO MOS CIRCUITS

Chip design hierarchy - VLSI Design flow- Basic MOS transistors: Enhancement Mode transistor action, Depletion Mode transistor action-Basic steps of fabrication process of PMOS, NMOS, CMOS and Bi-CMOS-NMOS transistor current equation – second order effects.

NMOS & CMOS INVERTER AND LAYOUT

NMOS & CMOS inverter – Determination of pull up / pull down ratios – Body effect- threshold voltage-Latchup problem in CMOS circuits- latchup prevention -Design Rules and Layout: Lambda based and 2µm CMOS Design rules for wires, Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates-stick diagram.

CMOS LOGIC GATE DESIGN AND POWER DISSIPATION

NAND and NOR gates - Complex logic gates - Tri state circuits - Large FETs - Transmission gate and pass transistor logic – Static and dynamic power dissipation.

STORAGE ELEMENTS AND DYNAMIC LOGIC CIRCUITS

SR latch - Bit level register - D flip flop - Dynamic D flip flop - Static RAM cell - Clocked CMOS - Dynamic logic - Domino logic - SR logic - Dynamic memories.

VERILOG HDL

Basic concepts - Modules and ports - Structural modeling - Data flow modeling - Behavioral modeling - Switch level modeling - Test benches - Verilog code for: adders, subtractors, multiplexer, demultiplexer, encoder, decoder, priority encoder, comparator, D-Latch, D flip flop, shift register and counter.

Total (L: 45 T:0)=45 Periods

Course Outcomes: At the end of the course, the student should be able to:

- *Describe the basics of CMOS process technology.*
- *Classify the CMOS and NMOS logic gates design rules and Characteristics.*
- *Design the complex logic gates and estimate the power dissipation*
- *Describe various memory elements and types of logic design.*
- *Model the digital system using Verilog HDL.*

Text Books :

1. ın P. Uyemura, “Chip Design for Submicron VLSI: CMOS layout and simulation”, Cengage Learning India Private Ltd, 11th Indian Reprint 2013.
2. mir Palnitkar, “Verilog HDL A Guide to Digital Design and Synthesis”, Pearson Education,2nd Edition, 2010.

Reference Books :

1. il H.E. Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design”, Pearson Education Asia, 2nd Edition, 2005.
2. mran Eshraghian, Douglas A. Pucknell and SholehEshraghian, “Essentials of VLSI Circuits and Systems”, Prentice Hall of India Pvt Ltd,2013.
3. ayne Wolf, “Modern VLSI Design System-On-Chip”, PHI, 3rd Edition, 2007.
4. John P. Uyemura, “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, reprint 2009.
5. hasker, “Verilog HDL Primer”, BS publication, 3rd Edition 2005.
6. p://nptel.ac.in/courses/108101089/
7. p://nptel.ac.in/syllabus/syllabus.php?subjectId=117108041

K.S.R. COLLEGE OF ENGINEERING - TIRUCHENGODE- 637 215
(Autonomous)
Department of Electrical and Electronics Engineering
Lesson Plan
Code/Subject: 16EC531 / BASICS OF VLSI DESIGN
Year/Sem: III/V **Regulation: 2016** **Staff Name: Mr.S.Senthilkumar**

Lecture	Topic	Hours	Teaching Aid	Source	Page No
UNIT – INTRODUCTION TO MOS TRANSISTOR					
L01	Chip design hierarchy ,VLSI Design flow	01	BB	T1	17-20
L02	Basic MOS transistors: Enhancement Mode transistor action, Depletion Mode transistor action	01	BB	R6	Lec-12-13
L03	Fabrication steps of NMOS	01	BB/LCD	R7	Lec-12(pdf)
L04	Fabrication steps of PMOS	01	BB/LCD	R7	Lec-13(pdf)
L05	Fabrication steps of CMOS	01	BB/LCD	T1	43-52
L06	Fabrication steps of BiCMOS	01	BB/LCD	R6	Lec-40
L07	NMOS transistor current equation	01	BB	T1	121-123
L08 L09	Second order effects	02	BB	R1	51-60
	TOTAL	**09**			
UNIT – II NMOS AND CMOS INVERTER AND LAYOUT					
L01	NMOS inverter	01	B B	R2	38-40
L02	CMOS inverter	01	BB	R2	47-50
L03	Determination of pull up / pull down ratios	01	BB	R2	40-42
L04	Body effect- threshold voltage	01	BB	T1	124-125
L05	Latchup problem in CMOS circuits- latchup prevention	01	BB	R6	Lec-39
L06	Design Rules and Layout	01	BB	R1	83-90
L07	Lambda based and 2μm CMOS Design rules for wires,Contacts and Transistors	01	BB/LCD	T1	66-69
L08	Layout Diagrams for NMOS and CMOS Inverters and Gates	01	BB	R1	7-10
L09	Stick diagram	01	BB/LCD	R1	26-28
	TOTAL	**09**			
UNIT – III CMOS LOGIC GATE DESIGN AND POWER DISSIPATION					
L01 L02	NAND and NOR gates	02	B B	T1	169-180
L03	Complex logic gates	01	BB	T1	183-186
L04	Tri–state circuits	01	BB	T1	189-190
L05	Large FETs	01	BB	T1	190-193
L06	Transmission gate and pass transistor logic	01	BB	T1	193-197
L07	Static Power dissipation	01	BB	R1	129-131
L08 L09	Dynamic Power dissipation	01	BB	R1	131-135
	TOTAL	**09**			
UNIT – IV STORAGE ELEMENTS AND DYNAMIC LOGIC CIRCUITS					
L01	SR latch	01	B B	T1	221-224
L02	Bit level register	01	BB	T1	224-227
L03	D flip flop	01	BB	T1	227-228
L04	Dynamic D flip flop	01	BB	T1	228-233

L05	Static RAM cell	01	BB	T1	233-235
L06	Clocked CMOS	01	BB	T1	236-241
L07	Domino logic	01	BB	T1	241-244
L08	SR logic	01	BB	T1	244-246
L09	Dynamic memories	01	BB	T1	246-249
	TOTAL	**09**			
UNIT – V VERILOG HDL					
L01	Basic concepts- Modules and ports	01	B B	T2	49-57
L02	Structural gate level modeling	01	BB	T2	63-85
L03	Data flow modeling	01	BB	T2	89-116
L04	Behavioral modeling	01	BB	T2	119-137
L05	Switch level modeling & Test benches	01	BB	T2	171-185
L06	Verilog code for: Adders, Subtractors, Multiplexer, Demultiplexer	01	BB	T2	80-85
L07	Verilog code for: Encoder, Decoder, Priority Encoder, Comparator	01	BB	T2	101-115
L08 L09	Verilog code for: D–Latch, D flip flop, Shift register Counter	02	BB	T2	159-162
	TOTAL	**09**			

Teaching Aid:

1. BB - Black Board. LCD - LCD Projector. OHP - Over Head Projector.
2. Media - Multimedia. Model - Physical Mode**.**

Text Books:

1. John P. Uyemura, Chip Design for Submicron VLSI: CMOS layout and simulation, Cengage Learning India Private Ltd, 6th Indian Reprint2010.
2. Samir Palnitkar, Verilog HDL A Guide to Digital Design and Synthesis, 2nd edition, Pearson Education,2008.

References Books:

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education 4th edition,2011.
2. Kamran Eshraghian, Douglas A. Pucknell and Sholeh Eshraghian, Essentials of VLSI Circuits and Systems, Prentice Hall of India Pvt Ltd,2013.
3. Wayne Wolf, Modern VLSI Design System–On–Chip, PHI, 3rd edition,2007.
4. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons,2002.
5. Bhasker.J, Verilog HDL Primer, BS publication,2002.
6. http://nptel.ac.in/courses/108101089/108108111
7. http://nptel.ac.in/syllabus/syllabus.php?subjectId=117108041

UNIT I

INTRODUCTION TO MOS TRANSISTOR (CO1)

1. **What are four generations of Integration Circuits?** (Remembering)
   SSI (Small Scale Integration) , MSI (Medium Scale Integration) , LSI (Large Scale Integration) , VLSI (Very Large Scale Integration)
2. **Give the advantages of IC? (Remembering)**
   Size is less, High Speed, Less Power Dissipation
3. **Give the variety of Integrated Circuits? (Remembering)**
   More Specialized Circuits, Application Specific Integrated Circuits (ASICs) , Systems- On-Chips
4. **Give the basic process for IC fabrication (Remembering)**
   Silicon wafer Preparation, Epitaxial Growth, Oxidation, Photolithography, Diffusion, Ion Implantation, Isolation technique, Metallization, Assembly processing & Packaging
5. **What are the various Silicon wafer Preparation? (Remembering)**
   Crystal growth & doping, Ingot trimming & grinding, Ingot slicing, Wafer polishing & etching, Wafer cleaning.
6. **Different types of oxidation? (Remembering)**
   Dry & Wet Oxidation
7. **What is the transistors CMOS technology provides? (Remembering)**
   N-type transistors & p-type transistors.
8. **What are the different layers in MOS transistors? (Remembering)**
   Drain, Source & Gate
9. **What is Enhancement mode transistor? (Remembering)**
   The device that is normally cut-off with zero gate bias.
10. **What is Depletion mode Device? (Remembering)**
    The Device that conduct with zero gate bias.
11. **When the channel is said to be pinched–off? (Understanding)**
    If a large V_{ds} is applied this voltage with deplete the Inversion layer. This Voltage effectively pinches off the channel near the drain.
12. **Give the different types of CMOS process? (Remembering)**
    P-well process, N-well process, Silicon-On-Insulator Process, Twin- tub Process
13. **What are the steps involved in twin-tub process? (Remembering)**
    Tub Formation, Thin-oxide Construction, Source & Drain Implantation, Contact cut definition, Metallization.
14. **What are the advantages of Silicon-on-Insulator process? (Remembering)**
    No Latch-up, Due to absence of bulk transistor structures is denser than bulk silicon.
15. **What is BiCMOS Technology? (Remembering)**
    It is the combination of bipolar technology & CMOS technology.
16. **What are the basic processing steps involved in BiCMOS process? (Remembering)**
    Additional masks defining P base region, N Collector area, Buried Sub collector (SCCD) , Processing steps in CMOS process
17. **What are the advantages of CMOS process? (Remembering)**
    Low power Dissipation, High Packing density, Bi directional capability
18. **What are the advantages of CMOS process? (Remembering)**
    Low Input Impedance, Low delay Sensitivity to load.
19. **What is the fundamental goal in Device modeling**? **(Remembering)**
    To obtain the functional relationship among the terminal electrical variables of the device that is to be modeled.

20. **Define Short Channel devices? (Remembering)**

Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. With short channel devices the ratio between the lateral & vertical dimensions are reduced.

21. **What is pull down device? (Remembering)**

A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

22. **What is pull up device? (Understanding)**

A device connected so as to pull the output voltage to the upper supply voltage usually V_{DD} is called pull up device.

23. **What is Latch –up? (Understanding)**

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{DD} and V_{SS} with disastrous results. Careful control during fabrication is necessary to avoid this problem.

24. **How do you prevent Latch up problem? (Understanding)**

Latch up problem may be prevented in two basic ways,

1. Latch up resistance CMOS process 2.Layouttechniques

25. **List any two types of layout design rules. (Remembering)**

λ- rule, μ- rule.

26. **What are the common materials used as mask? (Remembering)**

Photoresist , twin dioxide (SiO_2), Polisilicon (polycrystalline silicon), Silicon nitrate (SiN).

27. **Mention the four main CMOS technologies. (Remembering)**

N-well process, p-well process, twin tub process, silicon on insulator.

28. **Define Delay time(Remembering)**

Delay time, t_d is the time difference between input transition (50%) and the 50% output level. This is the time taken for a logic transition to pass from input to output.

29. **What are two components of Power dissipation? (Remembering)**

There are two components that establish the amount of power dissipated in a CMOS circuit. These are: **(i)**Static dissipation due to leakage current or other current drawn continuously from the power supply. **(ii)**Dynamic dissipation due to **a.** switching transient current, **b.** Charging and discharging of load capacitances.

30. **State any two differences between CMOS and Bipolartechnology**. (Understanding)

CMOS Technology	Bipolar technology
• Low static power dissipation • High input impedance (low drive current) • Scalable threshold voltage • High noise margin • High packing density • High delay sensitivity to load(fan-out limitations) • Low output drive current • Low g_m (g_m aV_{in}) • Bidirectional capability • A near ideal switching device	• High power dissipation • Low input impedance (high drive current) • Low voltage swing logic • Low packing density • Low delay sensitivity to load • High output drive current • High g_m (g_m ae_{Vin}) • High f_t at low current • Essentially unidirectional

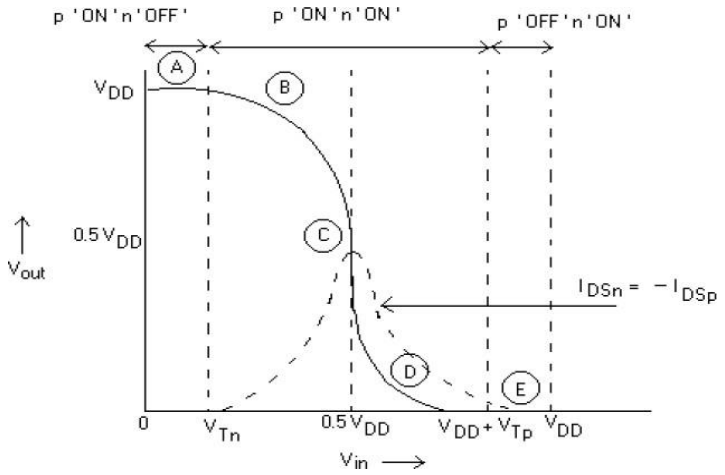
31. **Define rise time and fall time.** (Remembering)

Rise time t_r is the time for a wave form to rise from 10%to 90% of its steady state value. Fall time t_f is the time for a waveform to fall from 90% to 10% of its steady state value.

32. **Why NMOS technology is preferred more than PMOS technology? (Understanding)**
    NMOS transistors have greater switching speed when compared to PMOS transistors.
33. **What are the different operating regions foes an MOS transistor? (Remembering)**
    Cutoff region, Non- Saturated Region, Saturated Region
34. **What are the different MOS layers? (Remembering)**
    n-diffusion, p-diffusion, Polysilicon, Metal.
35. **Define Threshold voltage in MOS? (Remembering)**
    The Threshold voltage, V_T for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.
36. **What is Body effect? (Understanding)**
    The threshold voltage V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.
37. **What is Channel-length modulation? (Understanding)**
    The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied V_{DS}, increasing V_{DS} causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

UNIT – II
NMOS AND CMOS INVERTER AND GATES(C02)

1. **Give the CMOS inverter DC transfer characteristics and operating regions (Understanding)**



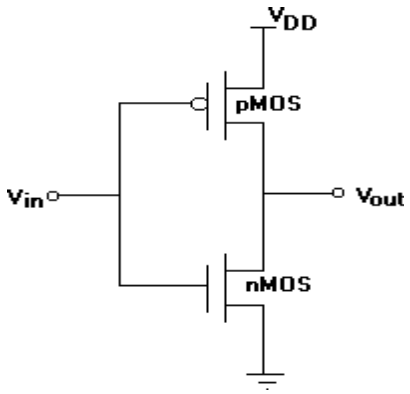
2. **What are design rules?** (Remembering)
   Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.
3. **What is CMOS latch up? How it can be prevented? (Understanding)**
   The MOS technology contains a number of intrinsic bipolar transistors. These are especially troublesome in CMOS processes, where the combination of wells and substrates results in the formation of p-n-p-n structures. Triggering these thyristor like devices leads to a shorting of V_{DD} & V_{SS} lines, usually resulting in a destruction of the chip.

   The remedies for the latch-up problem include:

   (i) An increase in substrate doping levels with a consequent drop in the value of R_{psubs}

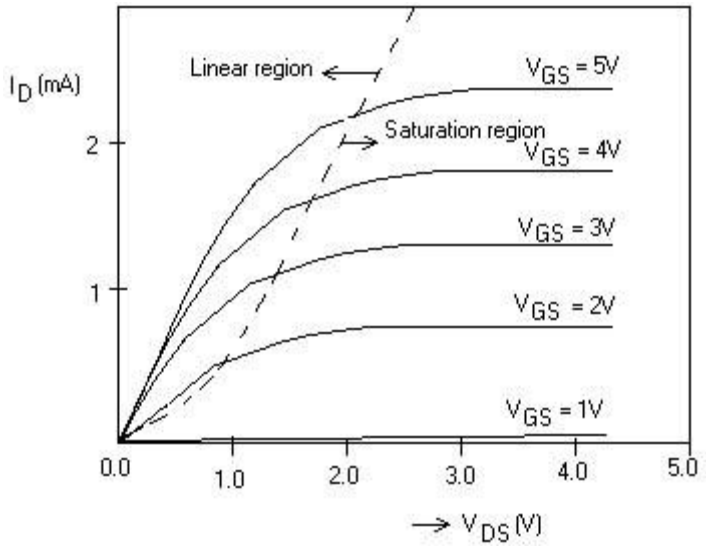
   (ii) Reducing R_{nwell} by control of fabrication parameters and ensuring a low contact resistance to V_{DD}.

   (iii) By introducing guard rings.
4. **Draw the circuit of a CMOS inverter. (Understanding)**



5. **What are the advantages of CMOS inverter over the other inverter configurations?** (Understanding)
   a. The steady state power dissipation of the CMOS inverter circuit is negligible.
   b. The voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0V and V_{DD}. This results in high noise margin.
6. **What are design rules? (Understanding)**
   Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.
7. **What are Lambda (λ) - based design rules? (Understanding)**
   These rules popularized by Mead and Conway are based on a single parameter λ, which characterizes the linear feature – the resolution of the complete wafer implementation process and permits first order scaling. They have been widely used, particularly in the educational context and in the design of multi project chips. In lambda based design rules, all paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process. Design rules, specify line widths, separations, and extensions in terms of λ .
8. **What is Stick Diagram? (Understanding)**
   It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.
9. **What are the uses of Stick diagram? (Remembering)**
   It can be drawn much easier and faster than a complex layout. These are especially important tools for layout built from large cells.
10. **Give the various color coding used in stick diagram? (Remembering)**
    Green – n-diffusion, Red- polysilicon, Blue –metal, Yellow- implant, Black-contact areas.
11. **What are the different regions of operation of a MOS transistor? (Understanding)**
    a. **Cut off region** :Here the current flow is essentially zero (accumulation mode)
    b. **Linear region**: It is also called weak inversion region where the drain current is dependent on the gate and the drain voltage w. r. to the substrate.
    c. **Saturation region**: Channel is strongly inverted and the drain current flow is ideally independent of the drain-source voltage (strong-inversion region).
12. **Give the expressions for drain current for different modes of operation of MOS transistor.**
    c. Cut off region: $I_D=0$ (Remembering)
    d. Linear region: $I_D = k_n [(V_{GS} – V_T) V_{DS} – V_{DS}2/2]$
    e. Saturation region: $I_D = (k_n /2) (V_{GS} –V_T)^2$
13. **What are the secondary effects of MOS transistor? (Remembering)**
    f. Threshold voltage variations
    g. Source to drain resistance
    h. Variation in I-V characteristics
    i. Subthreshold conduction
    j. CMOS latchup.

14. Plot the current-voltage characteristics of a nMOS transistor. (Understanding)



15. Define accumulation mode. (Remembering)

The initial distribution of mobile positive holes in a p type silicon substrate of a mos transistor for a voltage much less than the threshold voltage.

16. What are the static properties of complementary CMOS Gates? (Remembering)

a. They exhibit rails-to-rail swing with VOH = VDD and VOL =GND.

b. The circuits have no static power dissipation, since the circuits are designed such that the pull-down and pull-up networks are mutually exclusive.

c. The analysis of the DC voltage transfer characteristics and the noise margins is more complicated than for the inverter, as these parameters depend upon the data input patterns applied to the gate.

17. What are the major limitations associated with complementary CMO Sgate? (Remembering)

a. ThenumberoftransistorsrequiredtoimplementanNfan-ingateis2N.Thiscanresultin a significantly large implementation area.

b. The propagation delay of a complementary CMOS gate deteriorates rapidly as a function of the fan-in.

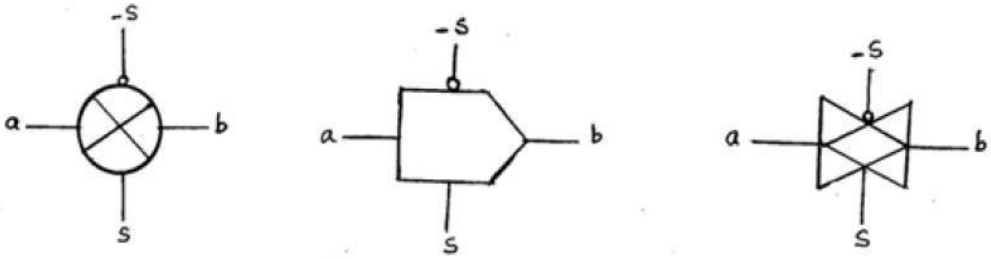
18. Define mobility variation(μ). (Remembering)

$$\mu = \frac{\boldsymbol{Average\ carrier\ drift\ velocity\ (V)}}{\boldsymbol{Electric\ field(E)}}$$

UNIT III

CMOS LOGIC GATE DESIGN AND PERFORMANCE ESTIMATION(C03)

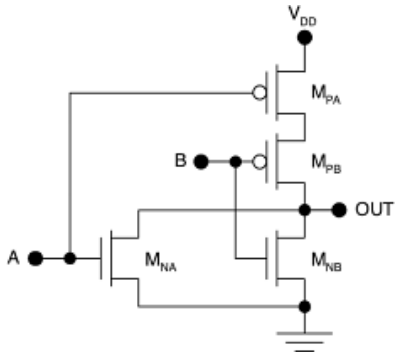
1. **Give the different symbols for transmission gate. (Remembering)**



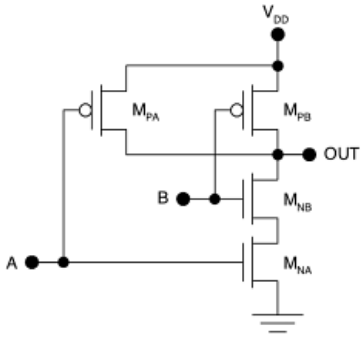
2. **What is a tri-state circuit?** (Remembering)

   A standard logic gate has outputs of 0 and 1. In tri-state circuit, the output can also be in a Hi-Z (high impedance) state, giving three distinct states.

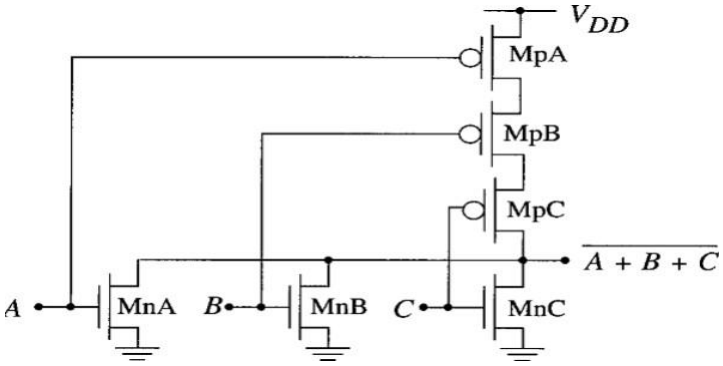
3. **Draw the CMOS NOR2 logic circuit.** (Apply)



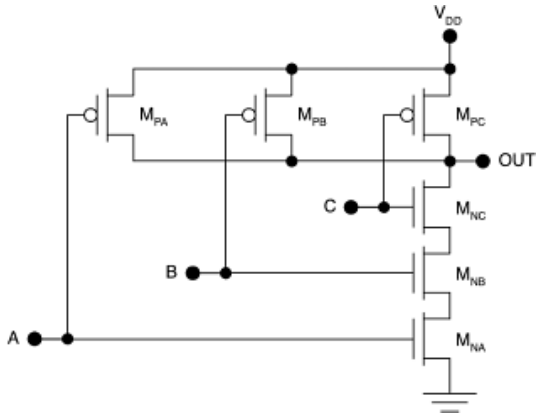
4. **Draw the CMOS NAND2 logic circuit.(Apply)**



5. **Draw the CMOS NOR3 logic circuit.(Understanding)**



6. **Draw the CMOS NAND3 logic circuit.(Understanding)**



7. **Define rise time and fall time.(Remembering)**
   Rise time- it is the time for signal to rise from a low value to the high value in a linear ramp. Fall time- it is the time interval for the pulse to fall from a high to a low value.
8. **Define time start and time pulse.(Remembering)**
   Time start- it is the delay from t=0 before the pulse is applied. Time pulse- it is the pulse width, i.e., the length of time that the pulse is kept at the high value.
9. **What are complex logic gates?(Remembering)**
   Complex logic gates give a combination of logical OR and AND functions in a single circuit. This CMOS feature is quite useful for merging functions and designing small circuits.
10. **What are the types of power dissipation?** (Remembering)
    - Static power dissipation (due to leakage current when the circuit idle).
    - Dynamic power dissipation(when the circuit is switching)and
    - Short –circuit power dissipation during switching of transistors.
11. **What is static power dissipation?** (Remembering)
    Power dissipation due to leakage current when the idle is called the static power dissipation. Static power due to
    - Sub – threshold conduction through OFF transistors
    - Tunneling current through gate oxide
    - Leakage through reverse biased diodes
    - contention current in radioed circuits.
12. **What is Dynamic power dissipation?** (Remembering)
    Power dissipation is due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called Dynamic power dissipation.

The Dynamic power dissipation at a particular output node is given by

$$Pd=CL\ Vdd^2\ Fclk\ .\ a$$

Where, CL = load capacitance ; a = activity factor ;Vdd =power supply ; Fclk= operating frequency

13. **What are the methods to reduce dynamic power dissipation?** (Remembering)
    - Reducing the product of capacitance and its switching frequency.
    - Eliminate logic switching that is not necessary for computation.
    - Reduce activity factor Reduce supply voltage
14. **What are the methods to reduce static power dissipation?** (Remembering)

    By selecting multi threshold voltages on circuit paths with low-Vt transistors while leakage on other paths with high-Vt transistors. By using two operating modes, active and standby for each function blocks. By adjusting the body bias (i.e) adjusting FBB (Forward Body Bias)in active mode to increase performance and RBB (Reverse Body Bias) in standby mode to reduce leakage. By using sleep transistors to isolate the supply from the block to achieve significant leakage power savings.
15. **What is short circuit power dissipation?** (Remembering)

    During switching, both NMOS and PMOS transistors will conduct simultaneously and provide a direct path between Vdd and the ground rail resulting in short circuit power dissipation
16. **Define design margin?** (Remembering)

    The additional performance capability above required standard basic system parameters that may be specified by a system designer to compensate for uncertainties is called design margin. Design margin required as there are three sources of variation- two environmental and one manufacturing.
17. **Write the applications of transmission gate?** (Remembering)
    - Multiplexing element of path selector
    - A latch element Anunlock switch
    - Act as a voltage controlled resistor connecting the input and output.
18. **What is pass transistor?** (Remembering)

    It is a MOS transistor, in which gate is driven by a control signal the source (out), the drain of the transistor is called constant or variable voltage potential(in) when the control signal is high, input is passed to the output and when the control signal is low, the output is floating topology such topology circuits is called pass transistor.
19. **List the advantages of pass transistor?** (Remembering)
    - Pass transistor logic(PTL)circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption.
    - They do not have path VDD to GND and do not dissipate stand by power(static power
    - dissipation).
20. **What is transmission gate?** (Remembering)

    The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and ~~s,~~ when s is high than the transmission gates passes the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.
21. **Why low power has become an important issue in the present day VLSI circuit realization?**
    - In deep submicron technology the power has become as one of the most important issue because of Increasing transistor count the number of transistor is getting doubled in every 18 months based on moore's law
    - Higher peed of operation the power dissipation is proportional to clock frequency greater device leakage current in nanometer technology the leakage

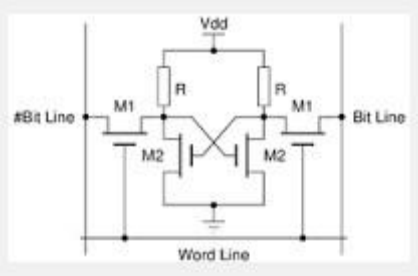
component become a significant percentage of the total power and the leakage current increases at a faster rate the dynamic power in technology generations.

22. **What are the various ways to reduce the delay time of a CMOS inverter?**
Various ways for reducing the delay time are given below: (Remembering)
    a) the width of the MOS transistor can be increased to reduce delay. this is known as gate sizing, which will be discussed later in more details.
    b) the load capacitance can be reduced to reduce delay. this is achived by using transistor of smaller and smaller dimension by feature generation technology.
    c) delay can also be reduced by increasing the supply voltage Vdd and/or reducing the threshold voltage Vt of the MOS transistors
23. **what makes dynamic CMOS circuits faster than static CMOS circuits?** (Remembering)
As MOS dynamic circuits require lesser number of transistor and capacitance is to be driven by it. this makes MOS dynamic circuits faster.
24. **what is glitching power dissipation?** (Remembering)
Because of finite delay of the gates used to realize boolean functions, different signals cannot reach the inputs of a gate simultaneously. this leads to spurious transition at the output before it settles down to its final value. the spurious transitions leads to charging and discharging of the outputs causing glitching power dissipation. It can be minimized by having balanced realization having same delay at the inputs.
25. **List various sources of leakage currents?** (Remembering)
Various source of leakage currents are listened below:
I1=Reverse-bias p-n junction diode leakage current. I2=band-to-band tunneling current I3=Sub threshold leakage current I4=Gate oxide tunneling current I7=Gate induced drain leakage current
26. **Compare and contrast clock gating versus power gating approaches.** (Remembering)
Clock gating minimizes dynamic power by stopping unnecessary transitions, but power gating minimizes leakage power by inserting a high Vt transistor in series with low Vt logic blocks.

UNIT – IV
STORAGE ELEMENTS AND DYNAMIC LOGIC CIRCUITS(CO4)

1. **What is called latch?(Remembering)**
   Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.
2. **List different types of flip-flops.(Remembering)**
   SR flip-flop ,Clocked RS flip-flop, D flip-flop, T flip-flop, JK flip-flop, JK master slave flip-flop.
3. **What do you mean by triggering of flip-flop.(Understanding)**
   The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop.
4. **What is an excitation table?(Remembering)**
   During the design process we usually know the transition from present state to next state and wish to find the flip-flop input conditions that will cause the required transition. A table which lists the required inputs for a given chance of state is called an excitation table.
5. **What is the operation of D flip-flop?(Remembering)**
   In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.
6. **What is a master-slave flip-flop?(Remembering)**
   A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.
7. **Define registers.(Remembering)**
   A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.
8. **Define Static RAM and dynamic RAM (Understanding)**
   Static RAM use flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.
9. **Define flip-flop (Remembering)**
   Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.
10. **What is SRAM?(Remembering)**
    Static Random Access Memories (SRAMs) are highly repetitive VLSI structures that are used for read/write data storage. An SRAM cell is different from a simple latch, in that it uses the same lines for input and output.
11. **What is a dynamic circuit?(Remembering)**
    A dynamic circuit operates by using the parasitic capacitance on a CMOS node to store electric charge.
12. **How dynamic flip-flop can be built?(Understanding)**
    A dynamic flip-flop can be built using two oppositely phased tri-state inverters.
13. **What is use of access transistors?(Remembering)**
    Access transistors are used to provide conduction path to the internal bit storage circuit.
14. **What is domino logic?(Remembering)**
    Domino logic is an extension that adds an inverter at the output to overcome the hardware glitch.

15. **Draw SRAM cell.(Understanding)**



16. **What is SR logic?(Remembering)**
    The domino circuit is designed to use the clock pulse to synchronize the pre charge event. Self-resetting logic (SR logic) uses a feedback network to automatically restore the charge on the internal capacitor after a discharge event.
17. **What are the advantages and applications of DRAM?(Remembering)**
    Dynamic RAMs (DRAMs) are most widely used memories because they can be manufactures at low cost at lowest cost per bit. System memories, such as those found in the motherboard of PC are DRAMs.
18. **What is ring oscillator? (Remembering)**
    A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain; the output of the last inverter is fed back into the first.

UNIT – V

VERILOG HDL(C05)

1. **What is Verilog HDL? (Remembering)**
   It is a hardware description language that can be used to model a digital system at Many levels of abstraction ranging from the algorithmic level to the gate level to the switch level.
2. **What are the various modeling used in Verilog?** (Remembering)
   Gate-level modeling, Data-flow modeling, Switch-level modeling, Behavioral modeling
3. **What is the structural gate-level modeling?** (Remembering)
   Structural modeling describes a digital logic networks in terms of the components that make up the system. Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.
4. **What is Switch-level modeling?** (Remembering)
   Verilog allows switch-level modeling that is based on the behavior of MOSFETs.
   Digital circuits at the MOS-transistor level are described using the MOSFET switches.
5. **What are identifiers?** (Remembering)
   Identifiers are names of modules, variables and other objects that we can reference in the design. Identifiers consists of upper and lower case letters, digits 0 through 9, the underscore character(_) and the dollar sign($). It must be a single group of characters. Examples: A014, a, b, in_o, s_out
6. **What are the value sets in Verilog?** (Remembering)
   Verilog supports four levels for the values needed to describe hardware referred to as value sets

Value levels	Condition in hardware circuits
0	Logic zero, false condition
1	Logic one, true condition
X	Unknown logic value
Z	High impedance, floating state

.

7. **What are the types of gate arrays in ASIC?** (Remembering)
   Channeled gate arrays, Channel less gate arrays, Structured gate arrays

8. **Give the classifications of timing control?** (Remembering)

Methods of timing control: 1.Delay-based timing control 2. Event-based timing control 3. Level-sensitive timing control

Types of delay-based timing control: 1. Regular delay control 2. Intra-assignment delay control 3. Zero delay control

Types of event-based timing control: 1. Regular event control 2. Named event control 3. Event OR control 4. Level-sensitive timing control

9. **Give the different arithmetic operators? (Remembering)**

Operator symbol	Operation performed	Number of operands
*	Multiply	Two
/	Divide	Two
+	Add	Two
-	Subtract	Two
%	Modulus	Two
**	Power (exponent)	Two

10. **What are the types of procedural assignments? (Remembering)**

1. Blocking assignment 2. Non-blocking assignment

11. **Give the different bitwise operators. (Remembering)**

Operator symbol	Operation performed	Number of operands
~	Bitwise negation	One
&	Bitwise and	Two
|	Bitwise or	Two
^	Bitwise xor	Two
^~ or ~^	Bitwise xnor	Two
~&	Bitwise nand	Two
~|	Bitwise nor	Two

12. **What are gate primitives? (Remembering)**

Verilog supports basic logic gates as predefined primitives. Primitive logic function keyword provides the basics for structural modeling at gate level. These primitives are instantiated like modules except that they are predefined in verilog and do not need a module definition. The important operations are and, nand, or, xor, xnor, and buf (non- inverting drive buffer).

13. **Give the two blocks in behavioral modeling. (Remembering)**

1. An initial block executes once in the simulation and is used to set up initial conditions and step-by-step dataflow
2. An always block executes in a loop and repeats during the simulation.

14. **What are the types of conditional statements?**

1. No else statement

Syntax: if ([expression]) true – statement;

2. One else statement

Syntax: if ([expression]) true – statement;
Else false-statement;

3. Nested if-else-if

Syntax: if ([expression1]) true statement 1;
Else if ([expression2]) true-statement 2;
Else if ([expression3]) true-statement 3;
Else default-statement;

The [expression] is evaluated. If it is true (1 or a non-zero value) true-statement is executed. If it is false (zero) or ambiguous (x), the false-statement is executed.

15. **Name the types of ports in Verilog**

Types of port	Keyword
Input port	Input
Output port	Output
Bidirectional port	inout

16. What are macros?

The logic cells in a gate-array library are often called macros.

17. Why do you require sensitivity list.

The list of events or signals expressed as an OR is known as a sensitivity list. A transmission on any one of multiple signals or events can trigger the execution of a statement or a block of statements.

18. What are two main data types of verilog HDL?

(1)Net data type (2) Register data type.

19. List out the classification of operators in verilog HDL.

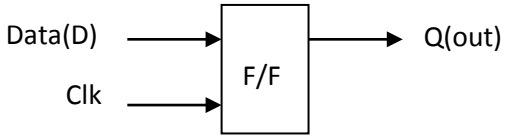
Types of operators are:

Arithmetic, relational, equality,logical,bitwise,reduction,shift,conditional,concatenation and replication operators.

20. Write the half adder program in verilog.

```
Module HA(s,c,a,b);
Input a,b;
Output s,c;
xor (s,a,b);
and (c,a,b);
end module;
```

21. Write the coding in verilog for the given block diagram. Use behavioural model.




```
Module DFF (Q,D,clk);
Input D,clk ;
Output Q;
reg Q;
always @ (pos edge clk)
 Q=D
 end module;
```

22. What is the difference between module and instance?

Module: basic building block

Instance: an instance of module has a unique identity and is different from other instance of the same module. Each instance has an independent copy of internals of module.

23. Give an example for implicit continuous assignments.

Drive values to a net

– assign out = a&b ; // and gate

– assign eq = (a==b) ; //comparator

– wire #10 inv = ~in ; // inverter with delay

– wire [7:0] c = a+b ; // 8-bitadder

24. Write the Verilog module for a 1 bit full adder.(Apply)

```
Module a(a, b, c, sum, carry);
input a,b,c;
output sum,carry;
wire d,e,f;
xor(sum,a,b,c);
and(d,a,b);
and(e,b,c);
and(f,a,c);
or(carry,d,e,f);
endmodule
```

25. What are the delay specification available in Verilog HDL for modeling a logic Gate Specify

propagation delay only (Understanding)

gatename #(prop_delay) [instance_name](output, in_1,in_2,…);

Specify both rise and fall times

gatename #(t_rise, t_fall) [instance_name](output, in_1,in_2,…);

Specify rise, fall, and turn-off times (tristate buffers)

gatename #(t_rise, t_fall, t_off) [instance_name](output,in_1, in_2,…);

26. Write the Verilog code to swap contents of two registers with/without a temporary register

With temp reg ; (Understanding)

```
always @ (posedge clock)begin
temp=b;b=a;a=temp;end
```

Without temp reg;

```
always @(posedge clock)begin
a <= b;b <= a;end
```

27. What are the difference between blocking and non-blocking assignments(Understanding)

The Verilog language has two forms of the procedural assignment statement: blocking and non-blocking. The two are distinguished by the = and <= assignment operators. The blocking assignment statement (= operator) acts much like in traditional programming languages. The whole statement is done before control passes on to the next statement. The non-blocking (<= operator) evaluates all the right-hand sides for the current time unit and assigns the left-hand sides at the end of the time unit.

```
module blocking;
reg [0:7] A, B;
initial begin: init1
A = 3;
#1 A = A + 1; // blocking procedural assignment
B = A + 1;
$display("Blocking: A= %b B= %b", A, B ); A = 3;
#1 A <= A + 1; // non-blocking procedural assignment
B <= A + 1;
#1 $display("Non-blocking: A= %b B= %b", A, B );
end
endmodule
```

28. What is meant continuous assignments in Verilog HDL?

Continuous assignments are the most basic assignment in dataflow modeling. Continuous assignments are used to model in combinational logic. It drives values into the nets.

Simplified Syntax

net [strength] [range] [delay] identifier = net or register ;

assign [strength] [delay] net = net or register ;

29. Give the design for defining the module? (Understanding)

```
Module design_name (portlist);
Input list;
Output list;
Inout list;
Endmodule
```

30. List out rules of identifiers?

- ✓ Can contain alphanumeric or underscore characters or dollar sign.
- ✓ May use any character by escaping with a black Slash at beginning of the identifier and terminating with whitespace.
- ✓ Can be upto 1024bytes
- ✓ Cannot contain whitespace

31. What is the difference between === and ==?(Understanding)

"==" it is logical equality.

"===" it is case equality.

output of "==" can be 1, 0 or X.

output of "===" can only be 0 or 1.

When you are comparing 2 nos using "==" and if one/both the numbers have one or more bits as "x" then the output would be "X" . But if use "===" outpout would be 0 or 1.

e.g A = 3'b1x0

B = 3'b10x

A == B will give X as output.

=== B will give 0 as output.

"==" is used for comparison of only 1's and 0's .It can't compare Xs. If any bit of the input is X output will be X

"===" is used for comparison of X also.

32. What is the difference between wire and reg? (Understanding)

Net types: (wire, tri)Physical connection between structural elements. Value assigned by a continuous assignment or a gate output. Register type: (reg, integer, time, real, real time) represents abstract data storage element. Assigned values only within an always statement or an initial statement. The main difference between wire and reg is wire cannot hold (store) the value when there no connection between a and b like a->b, if there is no connection in a and b, wire loose value. But reg can hold the value even if there in no connection. Default values: wire is Z,reg isx.

BIG QUESTIONS:

1. With neat diagrams explain the steps involved in the p-well process of CMOS fabrication.
2. With a neat diagram explain the steps involved in the n-well process of CMOS fabrication.
3. Describe in detail with neat sketches the Twin Tub method of CMOS fabrication.
4. Discuss the lambda based design rules for nMOS transistor.
5. With neat diagram of Latch-up effect in p-well structure explain Latch-up problem and the steps involved to overcome it.
6. Explain with neat diagrams the various CMOS fabrication technology.
7. Explain the latch up prevention techniques.
8. Explain with neat diagram the SOI process and mention its advantages.
9. Explain about CMOS interconnections with diagram.
10. Explain the design hierarchies.
11. Explain the operation of PMOS Enhancement transistor with neat diagram.
12. What is threshold voltage? Derive threshold voltage equation.
13. Explain the operation of NMOS Enhancement transistor with neat diagram.
14. Explain the Transmission gate and the tri state inverter briefly.
15. Explain about the various non ideal conditions in MOS device model.
16. Derive the expression for DC characteristics of CMOS inverter.
17. Explain the small signal AC characteristics of MOS transistor.
18. Derive the equation for threshold voltage of a MOS transistor and threshold voltage in terms of flat band voltage.
19. Derive the pull-up to pull down ratio for a nMOS inverter driven by another Nmos inverter.
20. Explain Pass transistor and Transmission gates with neat sketches.
21. Draw the stick and layout diagrams of an nMOS inverter.
22. Explain body effect in detail.
23. What are regions applicable in MOS transistor and write the equation?
24. Explain the transmission gate of nMOS pass transistor.
25. Explain tri state inverter with neat sketches.
26. What is latch? Explain in detail about its types and operation.
27. Explain in detail about bit level register.

28. Explain the operation of SR-latch and D-latch.
29. What is flip flop? Explain the operation of master-slave D-flip flop in detail.
30. Draw the architecture of dynamic DFF and Explain in detail.
31. Explain the read and write operations of static RAM cell with a CMOS circuit diagram. Draw its layout.
32. Explain in detail about dynamic logic and domino logic.
33. Write notes on SR logic and DRAMs. Explain read, write and hold operations performed by using CMOS SRAM cell.
34. Explain the functions of static RAM cell with its SPICE simulation.
35. ExplainbrieflyaboutthestructureofdynamicRAMcell.Howtheread,write, hold and refresh operations take place in a DRAM cell.
36. Design two input AND gate using DOMINO logic. Also explain how domino logic is cascaded with different function
37. Explain the concept involved in structural gate level modeling and also give the description for half adder and Full adder.
38. Write a verilog program for 3 to 8 decoder in gate level description.
39. What are the difference between behavioral and RTL modeling?
40. Write a verilog program for 8 bit full adder using one bit full adder. The one bit full adder should be written in behavioral modeling.
41. Explain in detail behavioral and RTL modeling.
42. Write the structural gate level description of decoder.
43. Explain the syntax of conditional statements in verilog HDL with examples.
44. Write the structural gate level description of equality detector.
45. Explain the concept of gate delay in VERILOG with example.
46. Write the structural gate level description of comparator.
47. Write the structural gate level description of priority encoder.
48. Explain the concept involved in Timing control in VERILOG.
49. Write the structural gate level description of D-latch.
50. Write the program using verilog HDL to implement a full adder circuit.
51. With a neat flow chart explain the VLSI design flow.
52. Write the structural gate level description of D flip flop.
53. Write a ripple carry adder program in verilog with the help of 1 bit full adder.
54. Explain gate level primitives and its design note.
55. Write the verilog program for the following using conditional and behavioral modeling.
    4 bit equality detector, ii. 4 bit magnitude comparator.

Reg. No. : | | | | | | | |

K.S.R. COLLEGE OF ENGINEERING, TIRUCHENGODE – 637 215

(AUTONOMOUS)

B. E. / B.Tech. DEGREE END SEMESTER EXAMINATION, APRIL / MAY - 2019

Fifth Semester

B.E. – ELECTRICAL AND ELECTRONICS ENGINEERING

16EC531 – Basics of VLSI Design

(Regulations 2016)

Time: Three hours **Maximum Marks: 100**

Answer ALL Questions

PART A — (10 x 2 = 20 Marks)

1.Make a difference between Enhancement mode and Depletion Mode MOS transistors.

2.What do you meant by Channel length modulation?

3.Draw the circuit diagram for two input NAND gate using CMOS transistors.

4.How to prevent Latch-Up problem?

5.Implement 2-input XOR gate using transmission gate logic

6.Implement a 2:1 multiplexer using pass transistor.

7.Differentiate between clocked and Domino CMOS Logic.

8.List out the different types of dynamic memories

9.What is called behavioural modelling?

10.Write the Verilog Code for D flip-flop using behavioural level modelling.

PART B — (5 x 16 = 80 Marks)

11.	(a)	(i)	Derive the drain current of MOS device in different operating regions.	(8)
		(ii)	Analyze the second order effects in MOS devices.	(8)
			(OR)	
	(b)		Give a brief note on CMOS and PMOS fabrication steps with necessary diagram.	(16)
12.	(a)		Explain Complementary MOS inverter DC characteristics with neat diagram.	(16)
			(OR)	
	(b)		Develop the necessary stick diagram and layout for the design of NAND and NOR gates.	(16)
13.	(a)	(i)	Construct the following function using CMOS transistors F = (a. b + c. d. e)'	(8)
		(ii)	Illustrate the model of transmission gates with neat diagram.	(8)
			(OR)	
	(b)	(i)	Write short notes on static and dynamic power dissipation**.**	(8)
		ii)	Write short notes on tristate circuits	(8)
14.	(a)	(i)	Design a D-latch using transmission gate.	(8)
		(ii)	Evaluate a 1-bit dynamic inverting and non inverting register using pass transistor.	(8)
			(OR)	
	(b)		Describe about the 4T-SRAM and 1T-DRAM cell with neat diagram.	(16)
15.	(a)	(i)	Write the gate level structural description for 4-bit binary adders.	(8)
		(ii)	Write the Verilog code for 4to1 Multiplexer using behavioral level modeling.	(8)
			(OR)	
	(b)		Construct and write the Verilog code for universal shit registers using structural level modeling.	(16)

****